ABSTRACT

An ESD protection circuit is disclosed, including a silicon controlled switch (SCS), a switch control circuit, a metal oxide semiconductor field effect transistor (MOSFET), and a transistor control circuit, wherein when terminal over-voltage stress occurs over the positive power supply terminal in the active mode, the transistor control circuit is able to turn on the MOSFET, and at the same time the switch control circuit is able to trigger the SCS into conduction to form a discharging path, such that the terminal voltage over the positive power supply terminal will be rapidly decreased to the level of the holding voltage of the SCS to provide ESD protection for the IC. When terminal over-voltage stress in the active mode is removed, the MOSFET is disabled, but the SCS remains closed for discharge current, so the latch-up phenomenon is avoided.